SHRI SHANKARACHARYA TECHNICAL CAMPUS, BHILAI

(An Autonomous Institute affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION (Effective from 2020-2021 Batch)

M.Tech (Electronics & Telecommunication(VLSI Design)) Third Semester

S. No.	Board of Study	Subject	Subject Code	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1.	Electronics & Telecommunication	Analog VLSI	ET231301	3	1	-	100	20	20	140	4
2.	Refer Table- III		Elective - III	3	1	-	100	20	20	140	4
3.	Electronics & Telecommunication	Project	ET231391	-		28	100		100	200	14
4.	Electronics & Telecommunication	Seminar on Industrial Training	ET231392	-		3			20	20	2
Total				**6**	**2**	**31**	**300**	**40**	**160**	**500**	**24**

Table III

Elective-III			
Sr.No.	**Board of Study**	**Subject**	**Subject Code**
1	Electronics & Telecommunication	Algorithm for VLSI Design Automation	ET231321
2	Electronics & Telecommunication	ASIC Design	ET231322
3	Electronics & Telecommunication	Design of Semiconductor Memories	ET231323

.

			1.00	Applicable for AY 2021-22 Onwards
Chairman (AC)	Chairman (BoS)	Date of Release	Version	

SHRI SHANKARACHARYA TECHNICAL CAMPUS, BHILAI

(An Autonomous Institute affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION (Effective from 2020-2021 Batch)

M.Tech (Electronics & Telecommunication(VLSI Design)) Third Semester

Subject Code :ET231301	**Analog VLSI**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students able to acquire knowledge on Analog Circuit Design Using VLSI. The aim is to impart skills to students for explain Analog Circuit Design Using VLSI importance in the semiconductor industry and the various techniques.	On successful completion of the course, the student will be able to: CO1:-Understands the Basic current mirrors and single stage amplifiers CO2:-Analyze the Operational amplifier design CO3:-Analyze the Sample and hold circuits. CO4:-Understand the importance Data converters CO5:-Understand the basic Over sampling converters and filters

UNIT I **C01**

Basic current mirrors and single stage amplifiers – simple cmos current mirror – common source – common gate amplifier with current mirror active load – source flower with current mirror to supply bias current frequency response.**[5Hrs]**

UNIT – II **CO2**

Operational amplifier design and compensation: two stage CMOS operational amplifier – feedback and operational amplifier compensation – advanced current mirrors – folded-cascode operational amplifier – current mirror operational amplifier.Comparator – charge injection error – latchedcomparators – BiCMOS comparators..**[5Hrs]**

UNIT – III **CO3**

Sample and hold and switched capacitor circuits : MOS, cMOS and biMOS sample and hold circuits – switched capacitor circuits – basic operation and analysis first order and biquad filters – charge injection – switched**[5Hrs]**

UNIT – IV **CO4**

Data converters : ideal d/a and a/d converters – quantization noise – performance limitations. nyquist rate d/a converters – decoder based converters – binary scaled converters – hybrid converters. nyquist rate a/d converters – integrating – successive approximation folding and pipelined – a/d converters.**[5Hrs]**

			1.00	Applicable for AY 2021-22 Onwards
Chairman (AC)	Chairman (BoS)	Date of Release	Version	

UNIT – V **CO5**

Over sampling converters and filters : over sampling with and without noise haping – digital decimation filter – high order modulators – band pass over sampling converters – practical considerations – continuous time filters – mixers – PLLs - multipliers., **[5Hrs]**

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Analog Integrated Circuit Design	D.A. John and Ken Martin	1st Edition	John Wiley
2	Analog VLSI	Mohamed Ismail	1st Edition	Mc Graw hill

SHRI SHANKARACHARYA TECHNICAL CAMPUS, BHILAI

(An Autonomous Institute affiliated to CSVTU, Bhilai)

SCHEME OF TEACHING AND EXAMINATION (Effective from 2020-2021 Batch)

M.Tech (Electronics & Telecommunication(VLSI Design)) Third Semester

Subject Code ET231321	**Algorithm for VLSI Design Automation**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of Algorithm for VLSI Design Automation. Students will be able to understand about physical chip design, hierarchy, memory and memory element design concepts.	On successful completion of the course, the student will be able to: **CO1:-** Outline the features of Logic synthesis & verification. CO2:- understand VLSI automation Algorithms: Partitioning. CO3:- Analyze the Global Routing. CO4:- Understand the Detailed routing. CO5:- Design of Over the cell routing & via minimization.

UNIT- I: Logic synthesis & verification: **CO1**

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.. **[5Hrs]**

UNIT–II :VLSI automation Algorithms: **Partitioning:** **CO2**

problem formulation, classification of partitioning algorithms,
Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. **Placement, floor planning & pin assignment**: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.. **[5Hrs]**

UNIT – III: **Global Routing**: **CO3**

Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches. **[5Hrs]**

UNIT – IV: Detailed routing: **CO4**

problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. **[5Hrs]**

			1.00	Applicable for AY 2021-22 Onwards
Chairman (AC)	Chairman (BoS)	Date of Release	Version	

UNIT – V: Over the cell routing & via minimization : **CO5**

two layers over the cell routers, constrained & unconstrained via minimization. **Compaction:** problem formulation, one-dimensional compaction, two dimension-based compaction, hierarchical compaction. **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Algorithms for VLSI physical design Automation	Naveed Shervani	Second	Kluwer Academic Publisher
2	Introduction to CAD for VLSI"	Trimburger	-	Kluwer Academic publisher, 2002

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Algorithm and Data Structures for VLSI Design	Christophn Meinel & Thorsten Theobold	-	KAP, 2002.
2	Evolutionary Algorithm for VLSI	Rolf Drechsheler	Second	-